MC9S12C128
THE TIMER MODULE (TIM)

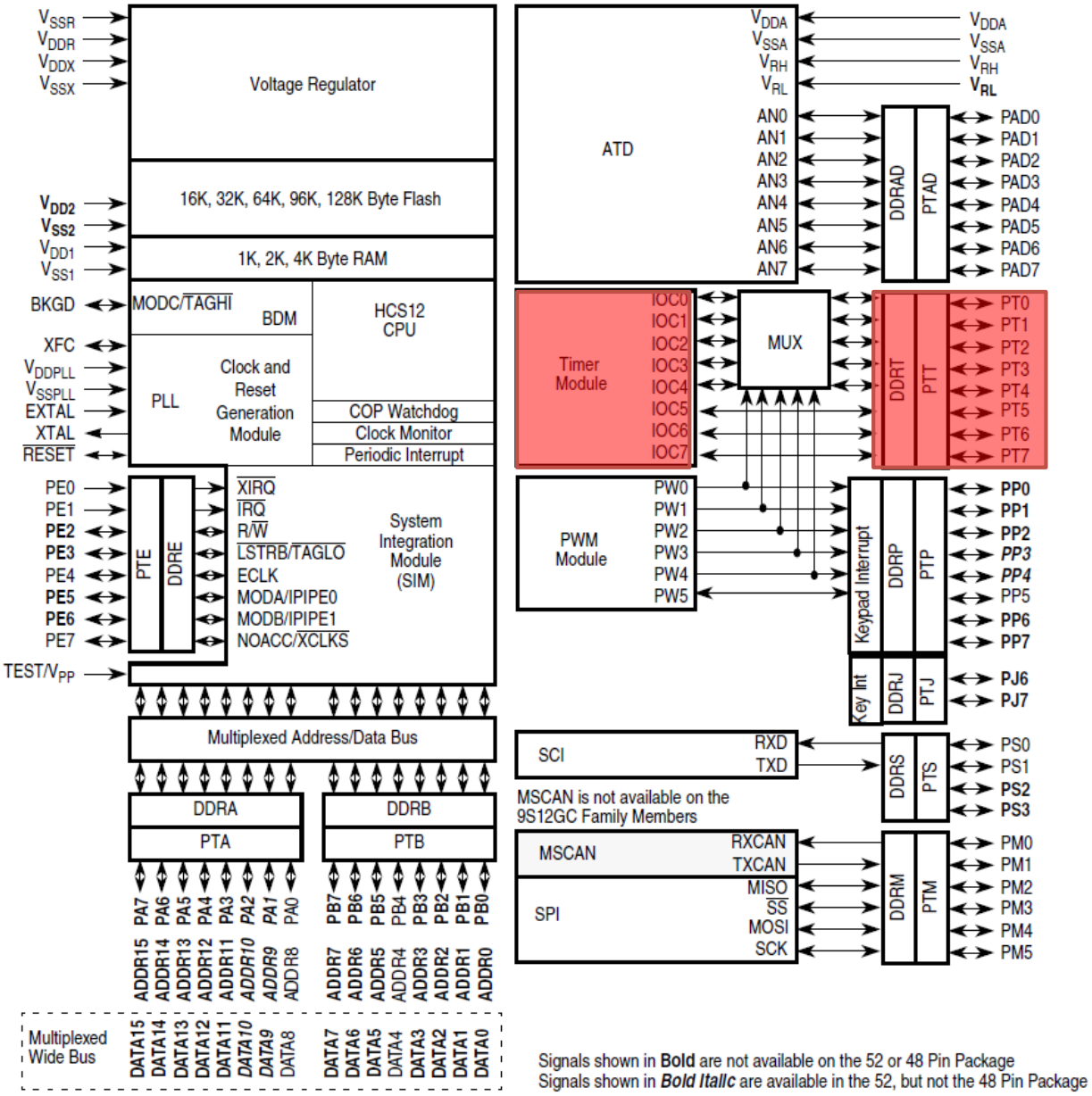
Timer Module

- input capture function
- output compare function
- pulse accumulator (event counter *or* gated time accumulator)

input capture function – detect a transition edge (conf.) and record the time.

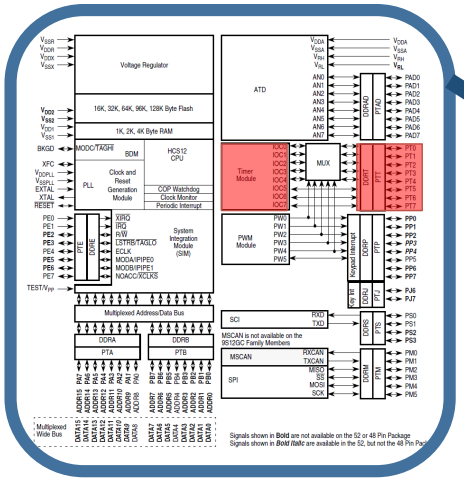
output compare function – start an action when the 16 bit counter reaches a certain value

pulse accumulator - measure external events marked as signal pulses on a corresponding pin



Based on fig. Figure 1-1. MC9S12C-Family / MC9S12GC-Family Block Diagram

MC9S12C Family MC9S12GC Family, Reference Manual



Bus clock

8MHz

Prescaler

16-bit Counter

Registers

16-bit
Pulse accumulator

Timer overflow interrupt

Timer channel 0 interrupt

Timer channel 7 interrupt

PA overflow interrupt

PA input interrupt

Channel 0
Input capture
Output compare
IOC0/PT0
PIN 5

Channel 1
Input capture
Output compare
IOC1/PT1
PIN 6

Channel 2
Input capture
Output compare
IOC3/PT2
PIN 7

Channel 3
Input capture
Output compare
IOC3/PT3
PIN 8

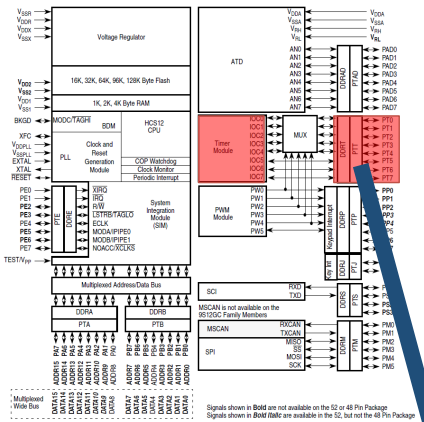
Channel 4
Input capture
Output compare
IOC3/PT4
PIN 11

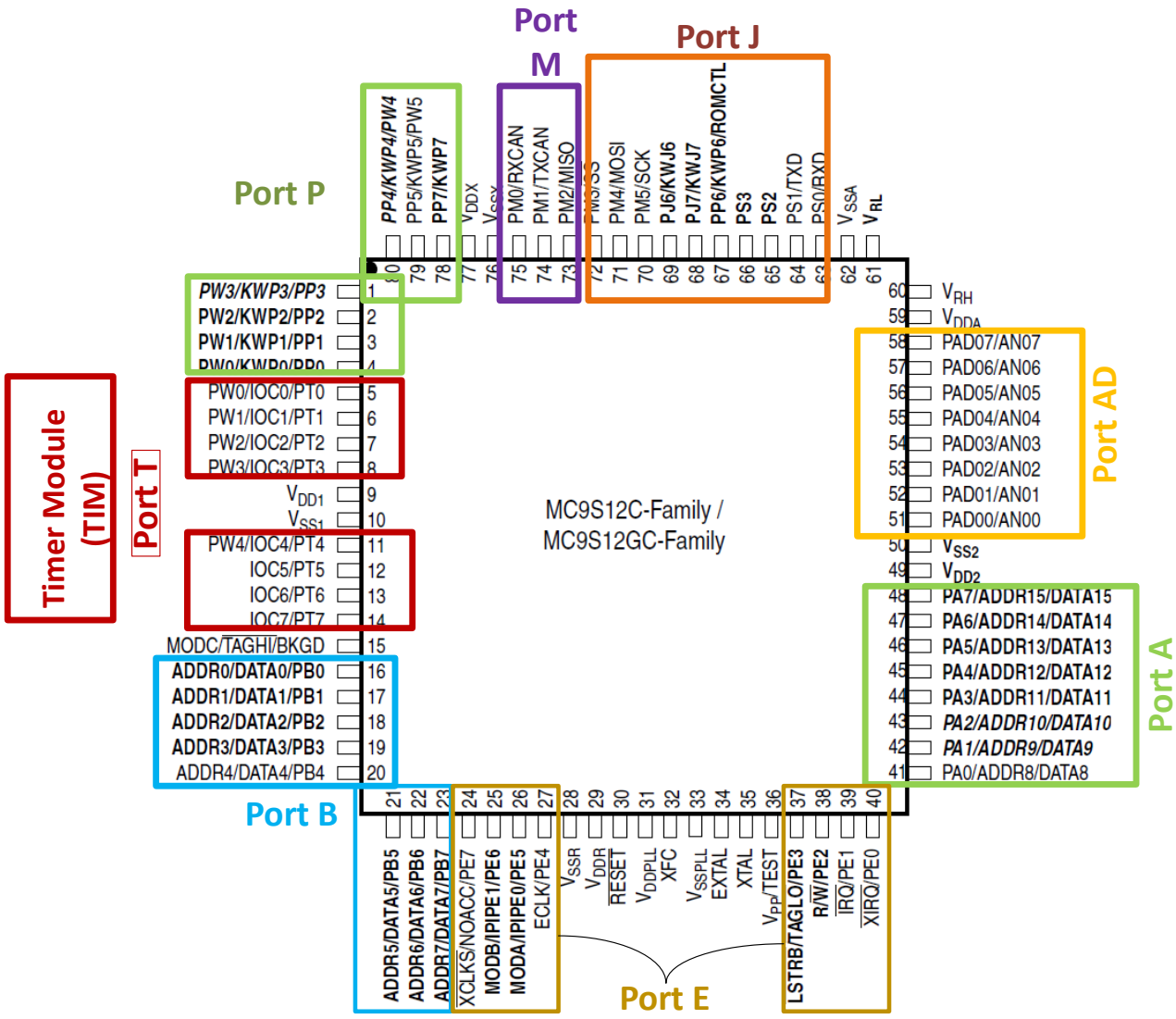
Channel 5
Input capture
Output compare
IOC3/PT5
PIN 12

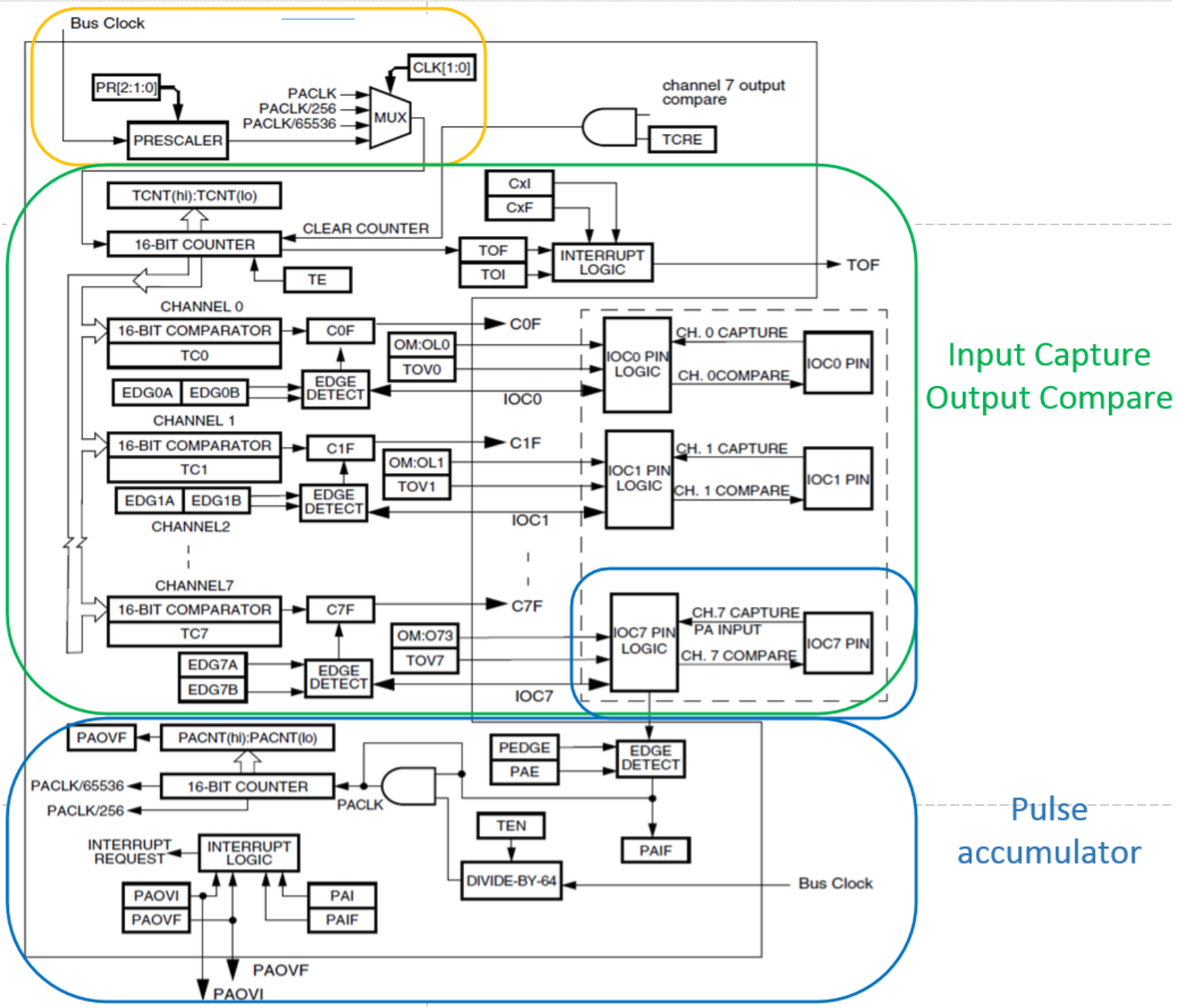
Channel 6
Input capture
Output compare
IOC6/PT6
PIN 13

Channel 7
Input capture
Output compare
IOC7/PT7
PIN 14

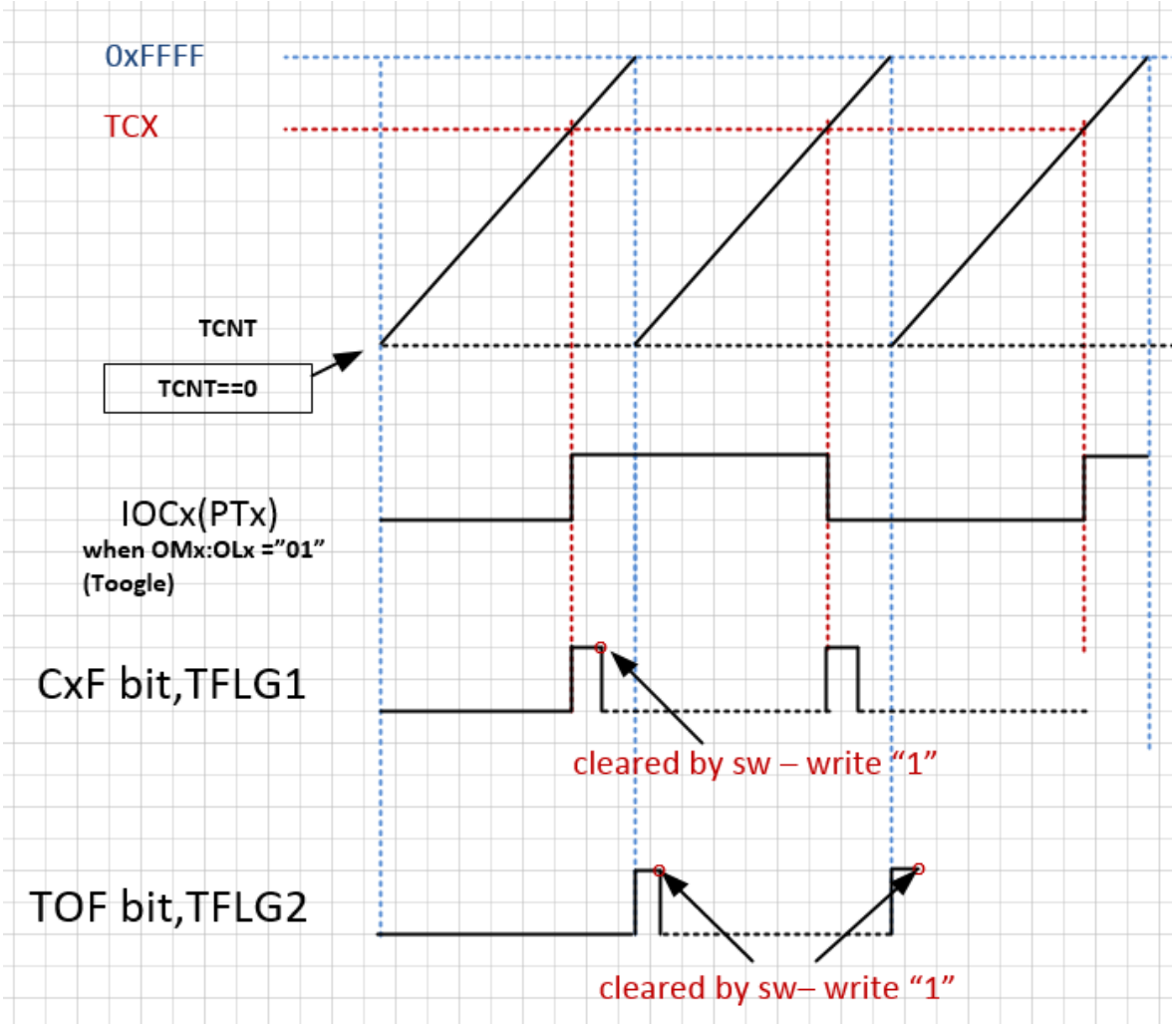
Figure 15-1. TIM16B8CV1 Block Diagram


Voltage Regulator
16K, 32K, 64K, 96K, 128K Byte Flash
1K, 2K, 4K Byte RAM
HCS12 CPU
BDM
Clock and Reset Generation Module
PLL
COP Watchdog
Clock Monitor
Periodic Interrupt
System Integration Module (SIM)
ATD
Timer Module
MUX
PWM Module
Keypad Interrupt
SCI
MSCAN
SPI
Multiplexed Address/Data Bus
DDRA
DDRB
PTA
PTB
Multiplexed Wide Bus
Signals shown in Bold are not available on the 52 or 48 Pin Package
Signals shown in Bold Italic are available in the 52, but not the 48 Pin Package


Timer Module (TIM)
Port T
Port P
Port M
Port J
Port AD
Port A
Port B
Port E
MC9S12C-Family / MC9S12GC-Family
PP4/KWP4/PW4
PP5/KWP5/PW5
PP7/KWP7
PM0/RXCAN
PM1/TXCAN
PM2/MISO
PM4/MOSI
PM5/SCK
PJ6/KWJ6
PJ7/KWJ7
PP6/KWP6/ROMCTL
PS3
PS2
PS1/TXD
PS0/RXD
PW3/KWP3/PP3
PW2/KWP2/PP2
PW1/KWP1/PP1
PW0/IOC0/PT0
PW1/IOC1/PT1
PW2/IOC2/PT2
PW3/IOC3/PT3
PW4/IOC4/PT4
IOC5/PT5
IOC6/PT6
IOC7/PT7
MODC/TAGHI/BKGD
ADDR0/DATA0/PB0
ADDR1/DATA1/PB1
ADDR2/DATA2/PB2
ADDR3/DATA3/PB3
ADDR4/DATA4/PB4
ADDR5/DATA5/PB5
ADDR6/DATA6/PB6
ADDR7/DATA7/PB7
XCLKS/NOACC/PE7
MODB/IPIPE1/PE6
MODA/IPIPE0/PE5
ECLK/PE4
RESET
XTAL
EXTAL
XFC
R/W/PE2
IRQ/PE1
XIRQ/PE0
PAD07/AN07
PAD06/AN06
PAD05/AN05
PAD04/AN04
PAD03/AN03
PAD02/AN02
PAD01/AN01
PAD00/AN00
PA7/ADDR15/DATA15
PA6/ADDR14/DATA14
PA5/ADDR13/DATA13
PA4/ADDR12/DATA12
PA3/ADDR11/DATA11
PA2/ADDR10/DATA10
PA1/ADDR9/DATA9
PA0/ADDR8/DATA8

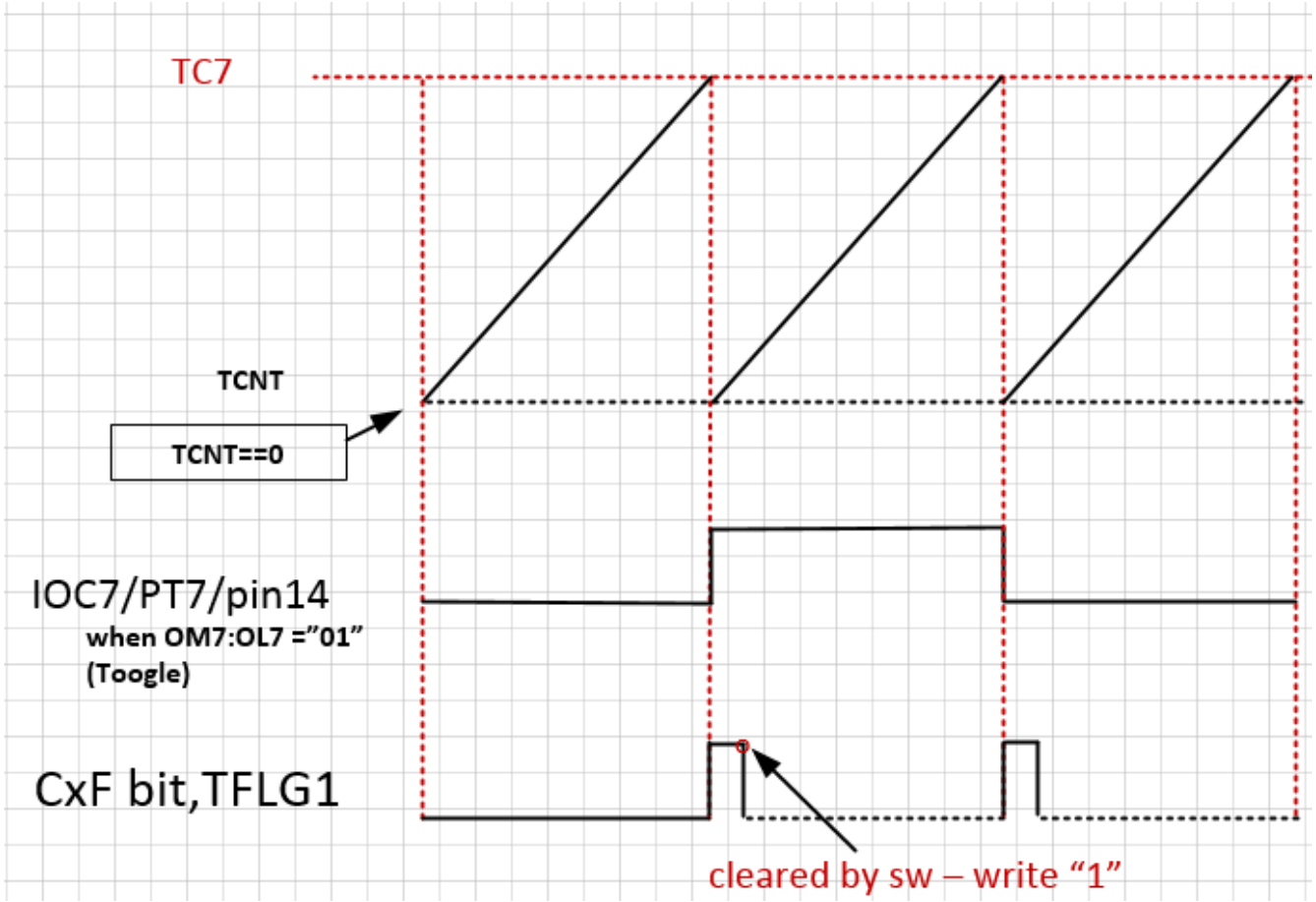

Bus Clock
PR[2:1:0]
PRESCALER
CLK[1:0]
PACLK
PACLK/256
PACLK/65536
MUX
channel 7 output compare
TCRE
TCNT(hi):TCNT(lo)
16-BIT COUNTER
CLEAR COUNTER
TE
CxI
CxF
TOF
TOI
INTERRUPT LOGIC
TOF
CHANNEL 0
16-BIT COMPARATOR
TC0
C0F
EDG0A
EDG0B
EDGE DETECT
OM:OL0
TOV0
C0F
IOC0
IOC0 PIN LOGIC
CH. 0 CAPTURE
CH. 0COMPARE
IOC0 PIN
CHANNEL 1
16-BIT COMPARATOR
TC1
C1F
EDG1A
EDG1B
EDGE DETECT
OM:OL1
TOV1
C1F
IOC1
IOC1 PIN LOGIC
CH. 1 CAPTURE
CH. 1 COMPARE
IOC1 PIN
CHANNEL2
CHANNEL7
16-BIT COMPARATOR
TC7
C7F
EDG7A
EDG7B
EDGE DETECT
OM:O73
TOV7
C7F
IOC7
IOC7 PIN LOGIC
CH.7 CAPTURE
PA INPUT
CH. 7 COMPARE
IOC7 PIN
PAOVF
PACNT(hi):PACNT(lo)
PACLK/65536
16-BIT COUNTER
PACLK/256
PACLK
PEDGE
PAE
EDGE DETECT
TEN
PAIF
INTERRUPT REQUEST
INTERRUPT LOGIC
PAOVI
PAOVF
PAI
PAIF
DIVIDE-BY-64
Bus Clock
PAOVF
PAOVI
Input Capture
Output Compare
Pulse
accumulator

output compare function – example 1



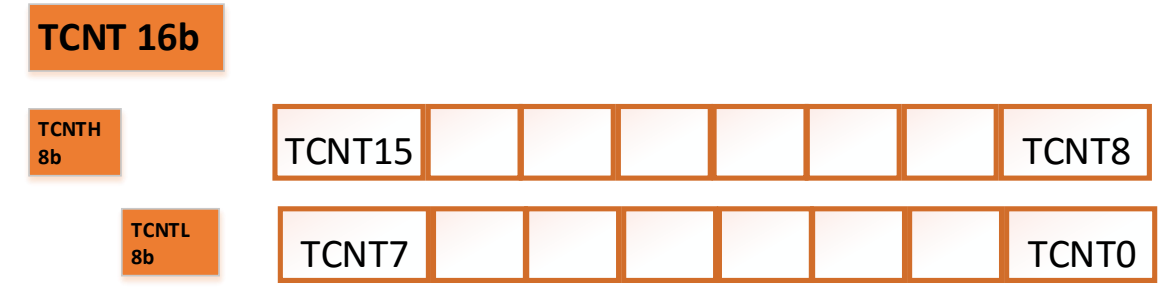
- Channel x in Output Compare Mode
  - **IOSx**="1", **TIOS** reg
- Action in case of channel x successful output compare is *toogle*
  - **OMx:OLx**="01", **TCTL1** || **TCTL2**

output compare function – example 2



- Channel x in Output Compare Mode
  - **IOS7**="1", **TIOS** reg
- Action in case of channel x successful output compare is *toogle*
  - **OM7:OL7**="01", **TCTL1** || **TCTL2**
- Reset the timer – TCNT at compare match with TC7
  - **TCRE** = '1' (Timer Counter Reset Enable), **TSCR2**

❑ **Timer Count Register (TCNT).**



- 16-bit main timer (func. as up counter)

❑ **Timer System Control Register 1 (TSCR1).**

TEN - Timer Enable

0 Disables the main timer, including the counter. Can be used for reducing power consumption.

1 Allows the timer to function normally.

❑ Timer System Control Register 2 (TSCR2)

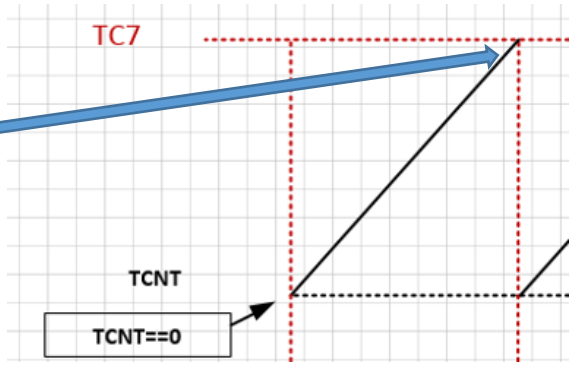
TSCR2 8b	TOI				TCRE	PR2	PR1	PR0

- **TOI – Timer Overflow Interrupt Enable.**

  "1" - generates an interrupt request when the TOF flag is set

- **TCRE - Timer Counter Reset Enable.**

  "1" - reset of the timer counter after a successful output compare 7 event



- **PR2,PR1,PR0- Timer Prescaler Select.**

  used for setting the prescaler value to derive the timer clock frequency from the bus clock (E-Clock)

PR2	PR1	PR0	Timer Clock
0	0	0	Bus Clock / 1
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

❑ Main Timer Interrupt Flag 2 (TFLG2)

TFLG2	TOF						

- **TOF - Timer Overflow Flag**

  is **SET** when the 16-bit counter overflows.

Common Registers for **input capture** and **output compare**

❑ Timer Input Capture/Output Compare Select (TIOS)

TIOS	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0

- **IOSx- Input Capture or Output Compare Channel Configuration**

  0 – channel x in INPUT CAPTURE; 1 – channel x in OUTPUT COMPARE

❑ Timer Interrupt Enable Register (TIE)

TIE	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I

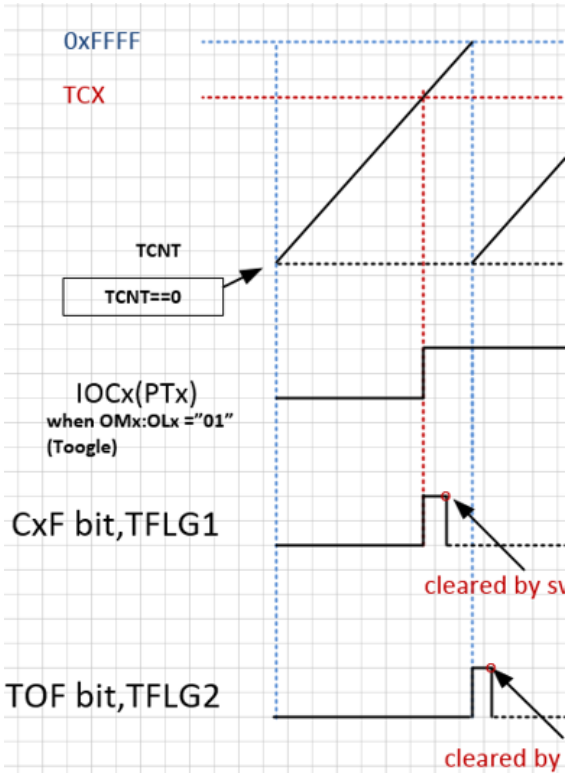
- **CxI - Input Capture/Output Compare "x" Interrupt Enable**

  "1" enables the interrupt for the corresponding channel

❑ Main Timer Interrupt Flag 1 (TFLG1)

TFLG1	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F

- **CxF - Input Capture/Output Compare Channel "x" Flag**
- **SET** when an input capture or output compare event occurs
- To CLEAR a flag CxF, write "1" to the CxF



❑ Timer Input Capture/Output Compare Registers 0-7 (TCx)

TCx								
TCxH 8b	bit15							bit8
TCxL 8b	bit7							bit0

- channel config. as **INPUT CAPTURE** - timer counter(**TCNT**) value latched when the event appears
- channel config. as **OUTPUT COMPARE** - condition value for output compare

Registers related to the **input capture** function

- **Timer Control Register 3 (TCTL3)**

- **Timer Control Register 4 (TCTL4)**

- **EDGnB EDGnA - Input Capture Edge Control**

  When channel n is set in INPUT CAPTURE mode, it configures the edge detection

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

Registers related to the **output compare** function

❑ Timer Control Register 1 (TCTL1), Timer Control Register 2 (TCTL2)

TCTL1	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
TCTL2	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0

- **OMx OLx** - encodes the output action in case of successful compare on channel x

OMx	OLx	Configuration
0	0	Timer disconnected from output pin logic
0	1	Toggle **OCx** (*PTx*) output line
1	0	Clear **OCx** (*PTx*) output line to zero
1	1	Set OCx output line to one

❑ Timer Compare Force Register (CFORC)

CFORC	FOC7	FOC06	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0

- **FOCx** - **Force Output Compare Action for Channel x**

  - FOCx set to 1 FORCES the output action (TCTL1 or TCTL2) on channel x to occur **immediately**

  - a **FORCED** action **does not set the flag (CxF-TFLG1) , does not trigger an interrupt**

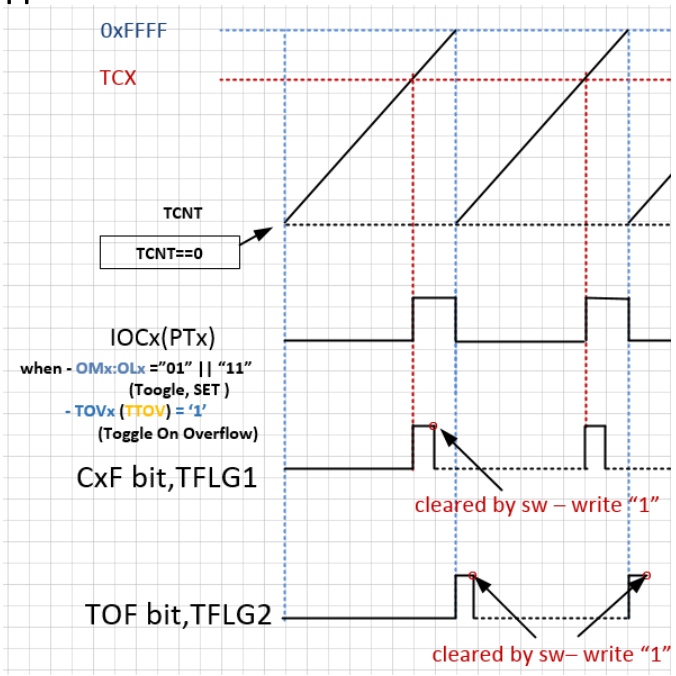
Registers related to the **output compare** function

❑ Timer Toggle On Overflow Register 1 (TTOV)

TTOV	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0

- **TOVx- Toggle On Overflow**

When **TOVx** is SET **Toogles** OCx (PTx) output line at **TCNT** overflow



❑ Output Compare 7 Mask Register (OC7M)

OC7M	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0

❑ Output Compare 7 Data Register (OC7D)

OC7D	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0

- Output compare function on channel 7 -- can control all 8 channels if config. in output compare mode
- **OC7Mx** selects the channels that are controlled by channel 7 output compare function
- **OC7Dx** configures the output value for each channel (when ch.7 controls that channel)