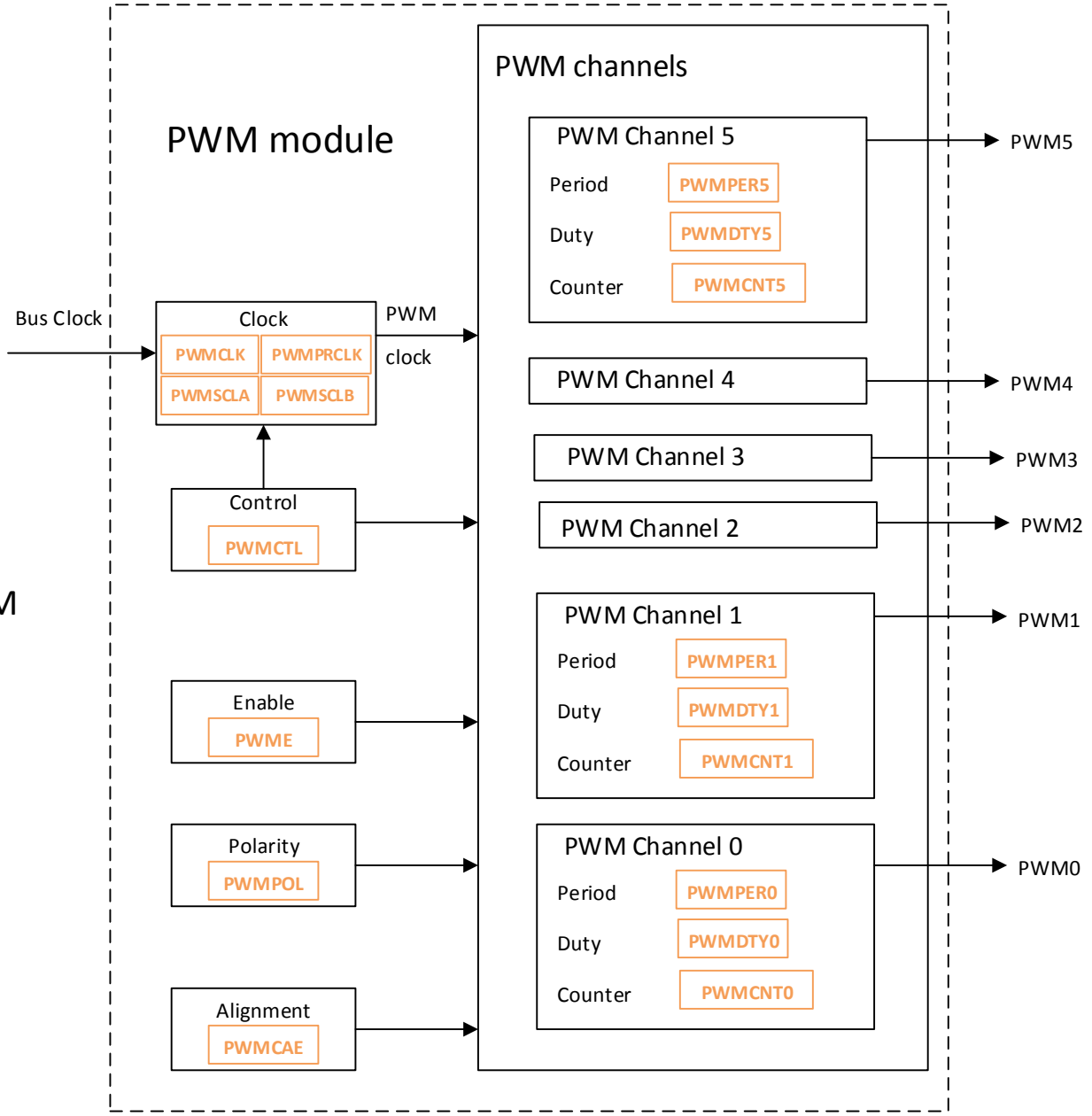
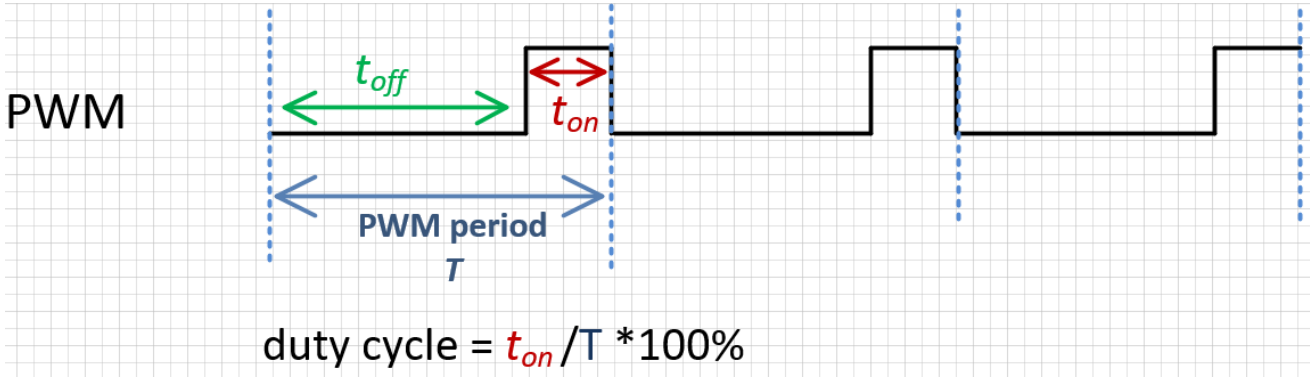
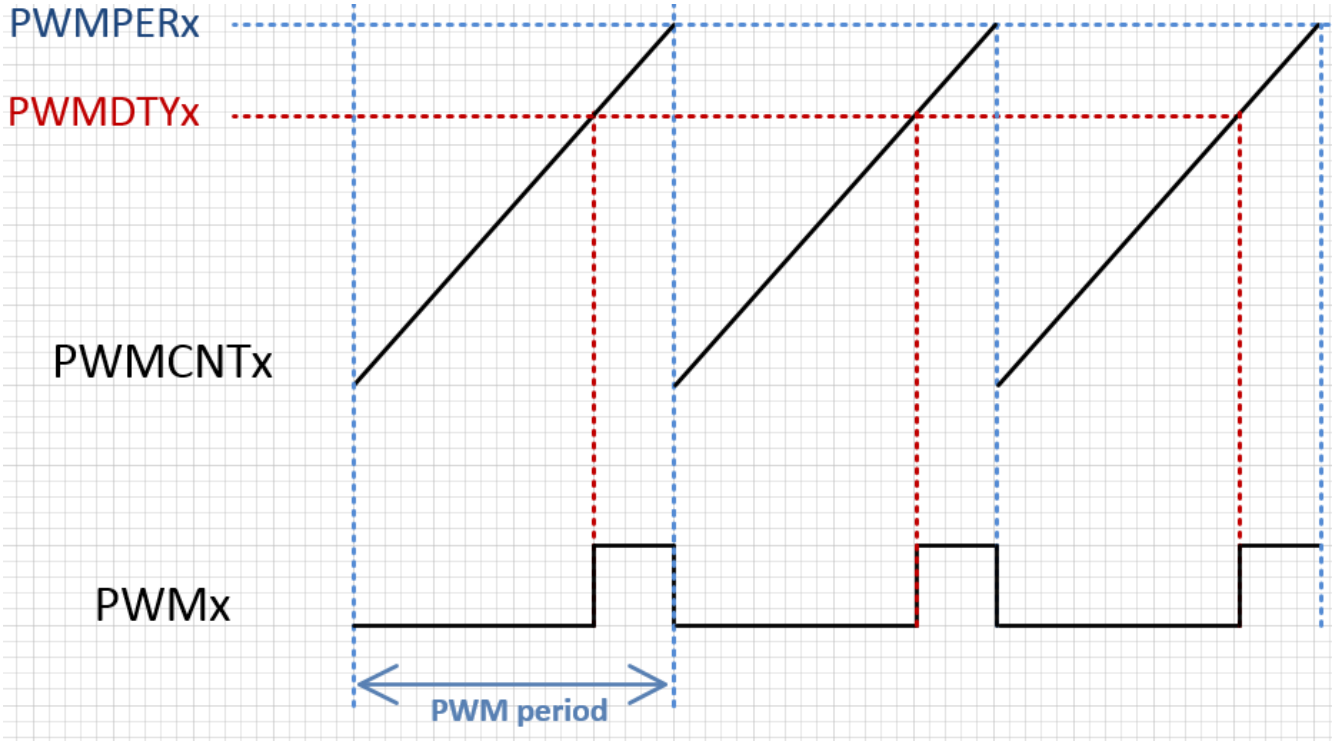
MC9S12C129 PULSE WIDTH MODULATION (PWM) MODULE

- 6x PWM channels(independent)
- Programmable frequency and duty cycle
- 8bit or 16bit PWM - 6x 8bit PWM channels or 3x16bit PWM mode
- four clock sources (two options on each channel)
- Center or left align outputs



GENERAL CONCEPTS





PWM module register synthesis

	Enable	Polarity	Clock	prescaler	alignment	8/16 bit	
PWM channel	PWME	PWMPOL	PWMCLK	PWMPRCLK	PWMCAE	PWNCTL	Output
PWM ch. 0	PWME0	PPOL0	PCLK0	PCKA2 PCKA1 PCKA0	CAE0	CON01	PWM0 - PTP0 Pin 4
PWM ch. 1	PWME1	PPOL1	PCLK1	PCKA2 PCKA1 PCKA0	CAE1	CON01	PWM1 – PTP1 Pin 3
PWM ch. 2	PWME2	PPOL2	PCLK2	PCKB2 PCKB1 PCKB0	CAE2	CON23	PWM2– PTP2 Pin 2
PWM ch. 3	PWME3	PPOL3	PCLK3	PCKB2 PCKB1 PCKB0	CAE3	CON23	PWM3 – PTP3 Pin 1
PWM ch. 4	PWME4	PPOL4	PCLK4	PCKA2 PCKA1 PCKA0	CAE4	CON34	PWM4 – PTP4 Pin 80
PWM ch. 5	PWME5	PPOL5	PCLK5	PCKA2 PCKA1 PCKA0	CAE5	CON34	PWM5 – PTP5 Pin 79

❑ PWM Enable Register (PWME)

PWME			PWME5	PWME4	PWME3	PWME2	PWME1	PWME0

- **PWMEx- Pulse Width Channel x Enable**

  0 – PWM channel x disabled; 1 – PWM channel x enabled

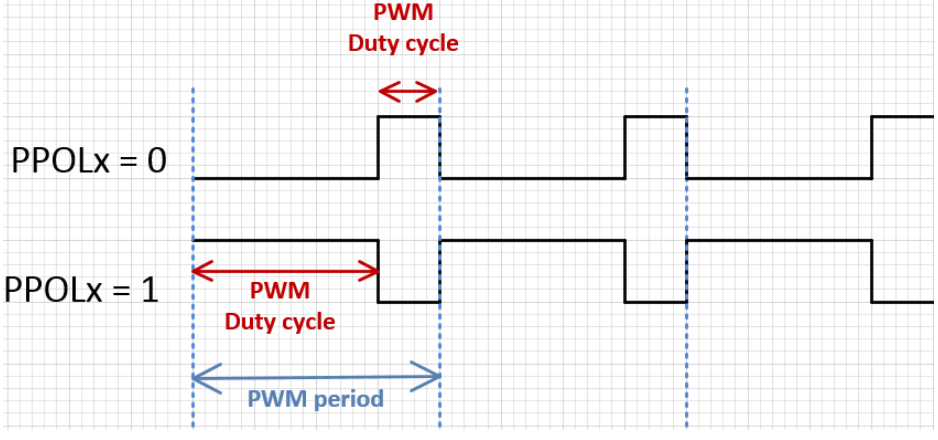
❑ PWM Polarity Register (PWMPOL)

PWMPOL			PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0

- **PWMEx- Pulse Width Channel x Polarity**

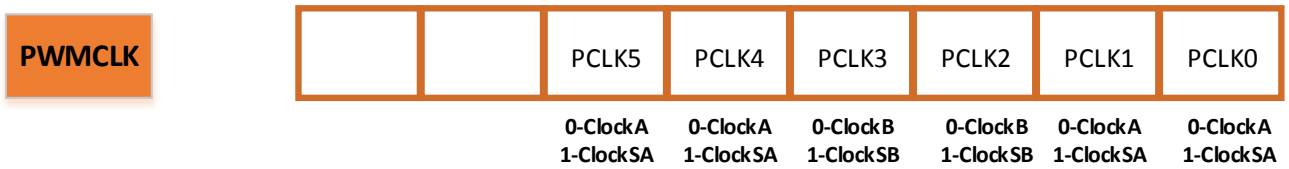
  0 – PWM channel x output starts on 0 at the beginning of the PWM period

  1 – PWM channel x output starts on 1 at the beginning of the PWM period



PWM Clock Registers

❑ PWM Clock Select Register (PWMCLK)



- **PCLKx- Pulse Width Channel x Clock Select**

  PCLK0, PCLK1, PCLK4, PCLK5 0 – ClockA ; 1 – ClockSA

  PCLK2, PCLK3 0 – ClockB ; 1 – ClockSB

❑ PWM Prescale Clock Select Register (PWMPRCLK)

- **PCKAx- Prescaler Select for Clock A**
- **PCKBx- Prescaler Select for Clock B**

PCKA2	PCKA1	PCKA0	Timer Clock
0	0	0	Bus Clock / 1
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

PWM Clock Registers

❑ PWM Scale A Register (PWMSCLA)

- Clock A is divided with a value between 2 and 512 with a 2 increment step
- Clock SA = Clock A / (2 * PWMSCLA)
- when PWMSCLA=0xFF => ClockSA = Clock A/(2*255)
- when PWMSCLA=0x00 => ClockSA = Clock A/(2*256)
- Clock SA can be selected as the clock sources for PWM channel 0, 1, 4 and 5.

❑ PWM Scale B Register (PWMSCLB)

- Clock SB can be selected as the clock sources for PWM channel 2 and 3.

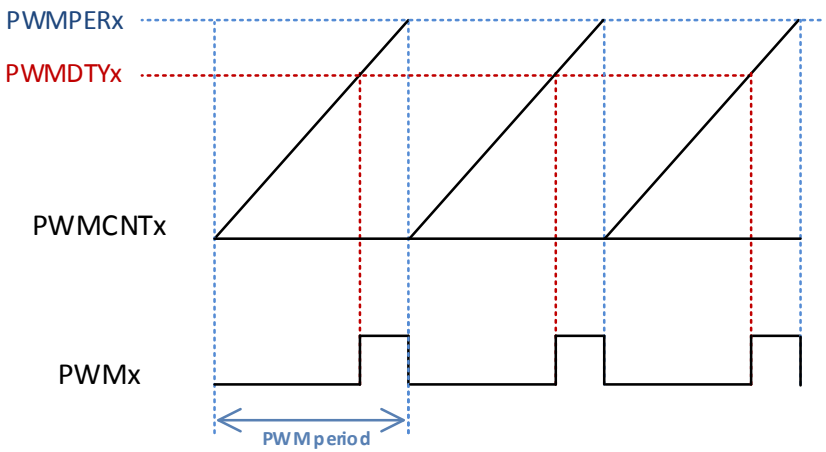
- PWM channel 0, 1, 4 and 5.
  - Clock A= Bus_clock / **PCKA[2:0]**
  - Clock SA = Clock A / (2 * **PWMSCLA**)
- PWM channel 2 and 3.
  - Clock B= Bus_clock / **PCKB[2:0]**
  - Clock SB = Clock B / (2 * **PWMSCLB**)

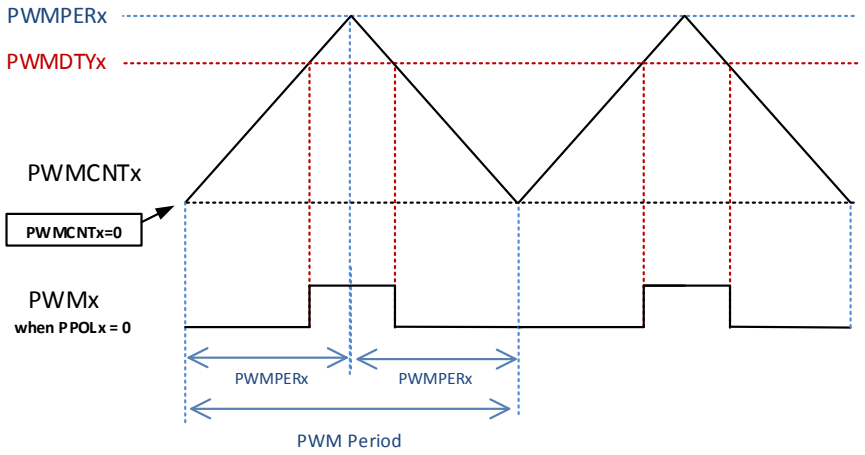
❑ PWM Center Align Enable Register (PWMCAE)

PWMCAE			CAE5	CAE4	CAE3	CAE2	CAE1	CAE0

- **CAEx- Center Aligned Output Mode on Channel x**

  0 – left PWM alignment , 1- center PWM alignment





Left alignment PWM waveform

Center alignment PWM waveform

❑ PWM Channel Counter Registers (PWMCNTx)

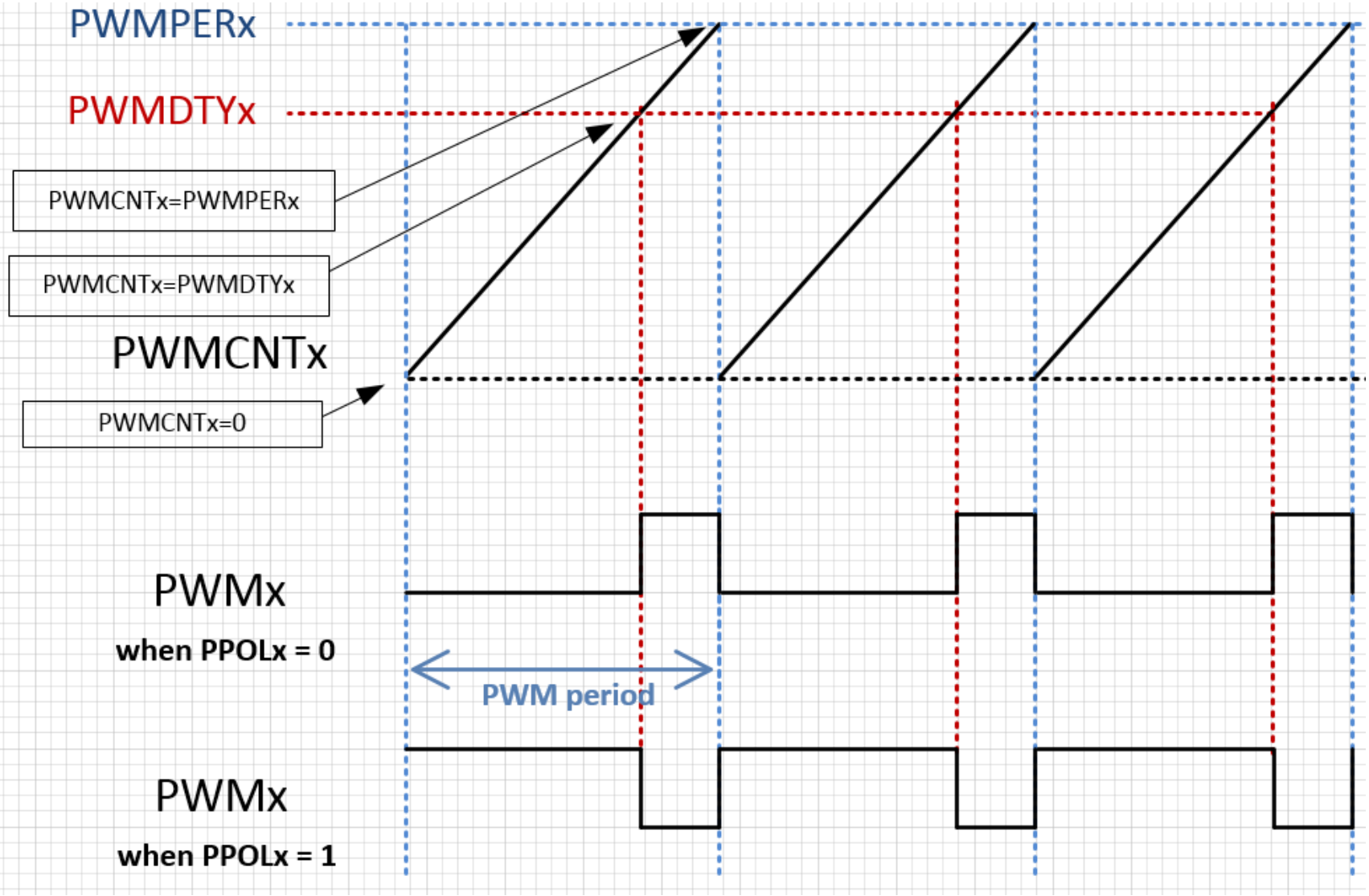
- configured as an up or **up/down counter** depending on the chosen PWM alignment mode (left aligned and center aligned)
- can be read at any time
- writing any value will
  - reset the counter to 0x00
  - set the counting mode to up
  - load the **duty register (PWMDTYx)** and the **period register (PWMPERx)** from the buffers

❑ PWM Channel Period Registers (PWMPERx)

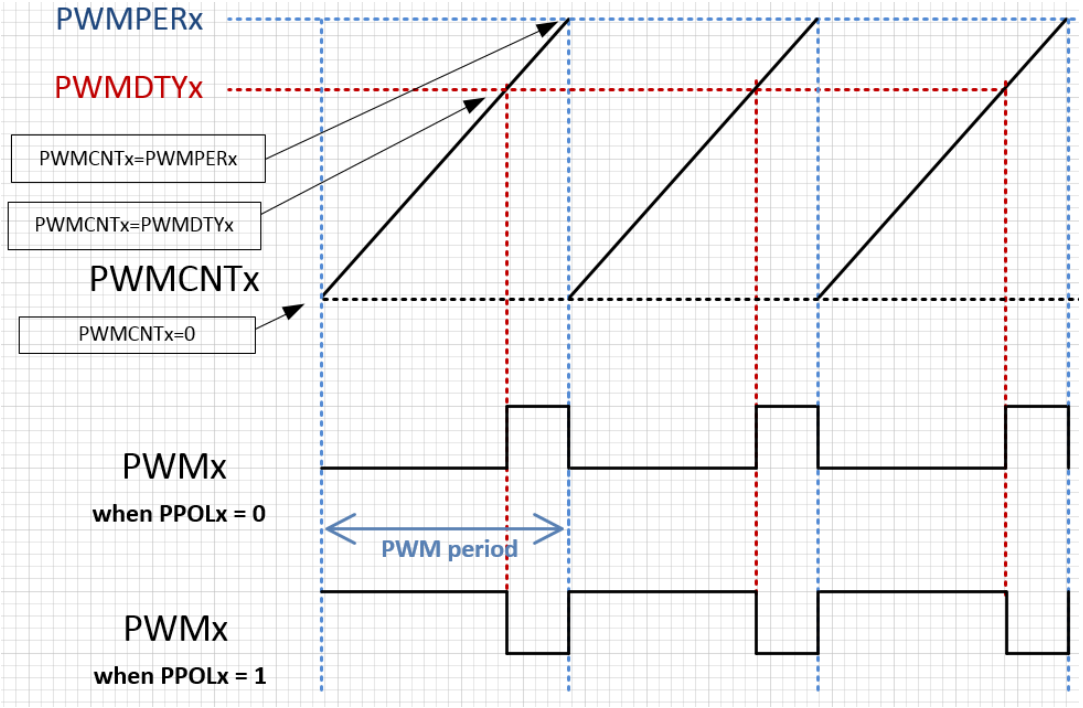
- 8 bit PWM Channel **Period** Register
- double buffered

❑ PWM Channel Duty Registers (PWMDTYx)

Left alignment PWM waveform



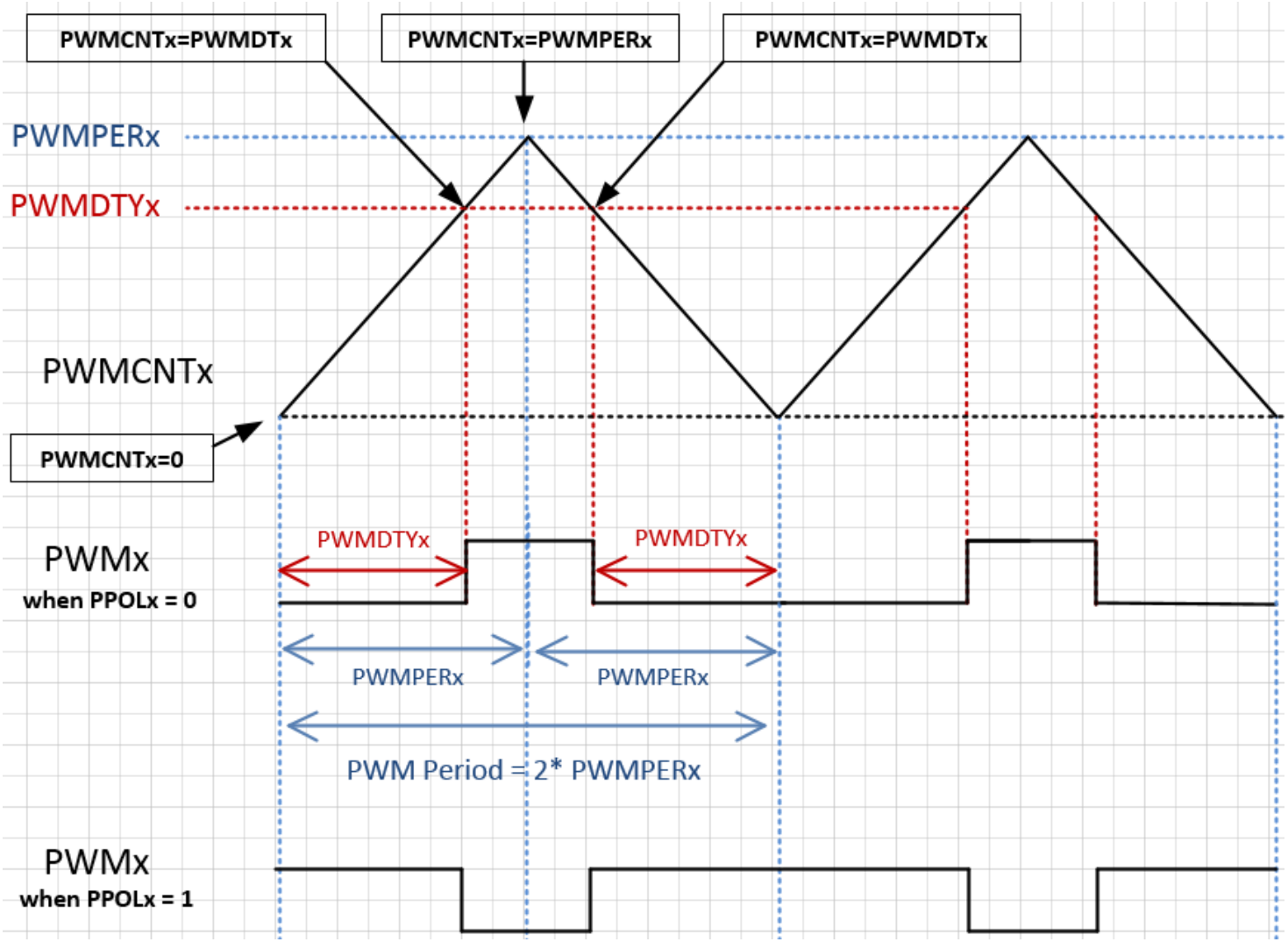
Left alignment PWM waveform



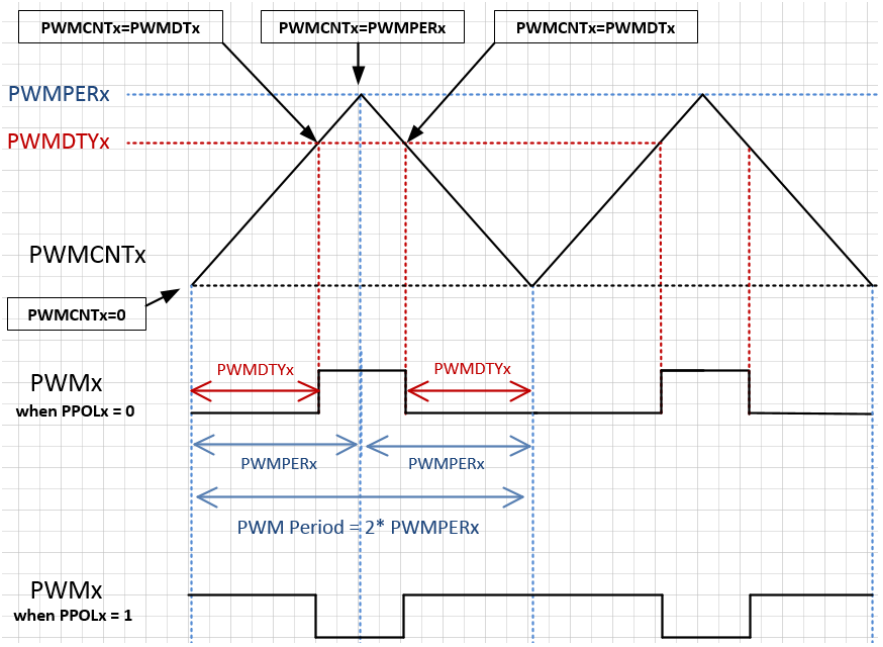
- PWMx frequency = ch_x_clock_frequency/**PWMPERx** ;
- PWMx period = ch_x_clock_period***PWMPERx** ;
- PWMx duty cycle= (**PWMPERx** - **PWMDTYx**)/ **PWMPERx** *100% (start polarity =0)

  PWMx duty cycle= (**PWMDTYx**)/ **PWMPERx** *100% (start polarity =1)

Center alignment PWM waveform



Center alignment PWM waveform

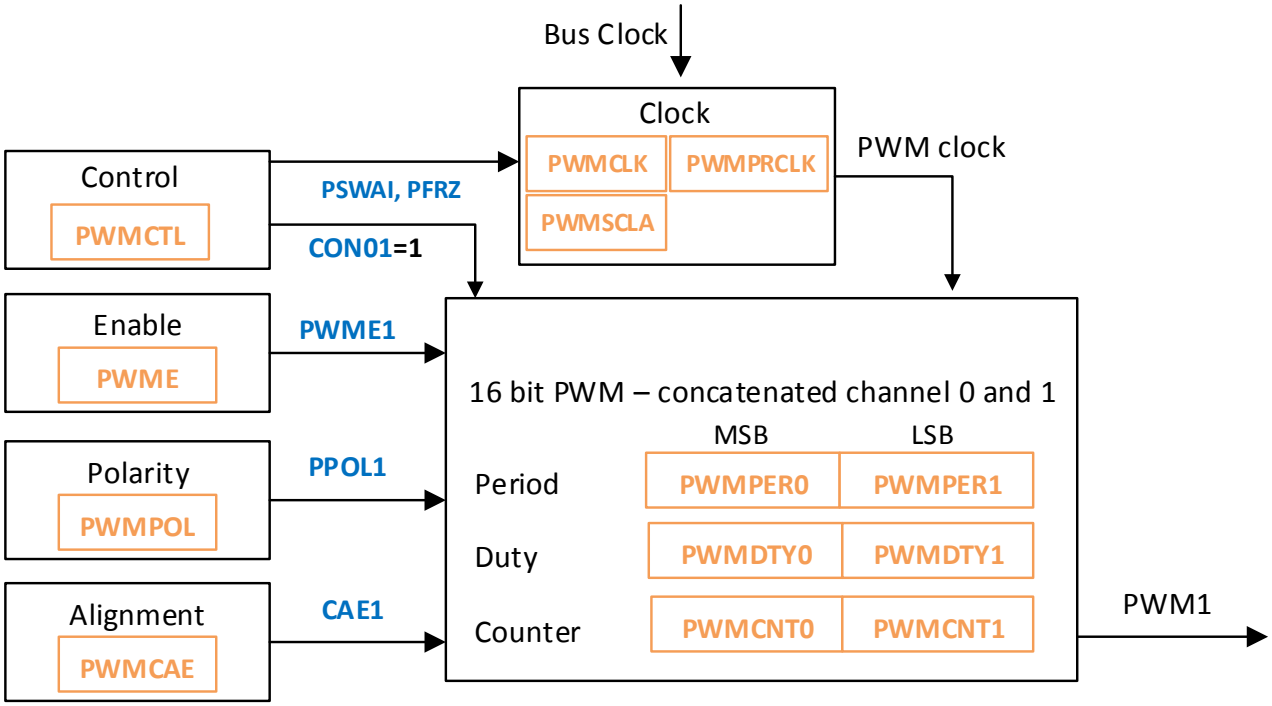


- PWMx frequency = ch_x_clock_frequency/(2 * **PWMPERx**) ;
- PWMx period = ch_x_clock_period***PWMPERx** * 2 ;

- PWMx duty cycle= (**PWMPERx** - **PWMDTYx**)/ **PWMPERx** *100% (start polarity =0)

  PWMx duty cycle= (**PWMDTYx**)/ **PWMPERx** *100% (start polarity =1)

16 BIT RESOLUTION PWM



PWNCTL	PWME	PWMPOL	PWMCLK	PWMPRCLK	PWMCAE	PWM Output
CON45	PWME5	PPOL5	PCLK5	PCKA2 PCKA1 PCKA0	CAE5	PWM5
CON23	PWME3	PPOL3	PCLK3	PCKB2 PCKB1 PCKB0	CAE3	PWM3
CON01	PWME1	PPOL1	PCLK1	PCKA2 PCKA1 PCKA0	CAE1	PWM1

PWM configuration bits for 16 bit PWM channels